

# Energy Analysis and Evaluation of WK-Recursive On-chip Interconnect

Mohamed Bakhouya  
 GSEM/SeT Laboratory  
 University of Technology of Belfort Montbeliard  
 90010 Belfort Cedex, France  
 Email : bakhouya@gmail.com

**Abstract**—With the increasing complexity of Multi-Core System-on-Chip (MCSoC) and its communications requirement, Network-on-Chip (NoC) has emerged as a solution of non-scalable shared bus schemes currently used in MCSoC implementation. Recently, a new NoC structure based on WK-recursive network was analyzed and compared to 2D Mesh structure based on several performance metrics such as packet losses, throughput, message delay, and network load. In this paper, we focus on the evaluation of energy consumption because of the importance of this feature in mobile systems that are typically battery-based systems and have to be energy efficient. A simple energy model is presented and simulation results are conducted to compare the Wk-recursive and 2D Mesh on-chip interconnects. The main objective is to provide the designer with initial insight on this network on-chip interconnect and the relationship between application traffics and energy consumption.

**Index Terms**—System-on-Chip, On-chip interconnect, Energy model, Workload models, Simulation and evaluation.

## I. INTRODUCTION

Emerging MCSoC for mobile systems are typically battery-based systems and have to support a wide range of streaming applications such as video and audio streams. Current interconnect architectures, used in MCSoCs to integrate Processing Elements (PEs), are based on the shared-medium bus-based schemes [1,2,3,4]. These schemes are limited because they are inherently non-scalable and produce large communication overhead that affects the performance and increases the energy consumption. New on-chip interconnects that are flexible as well as energy efficient are required. Recently, to meet these requirements, NoC paradigm has been proposed as a solution for the interconnect problem in MCSoC [5]. The main objectives are to increase the performance (e.g., delay, throughput), to optimize the resources usage and to minimize the energy consumption by separating the communication from the computation [6].

Different on-chip interconnect architectures based on packet-switching have been studied and adapted recently for MCSoC. Examples of these architectures are Fat-Tree [7], 2D Mesh [8], Ring [9], Butterfly-Fat Tree [10], Torus [5], Spidergon [15], Octagon [16], WK-recursive network [12,13]. It is worth noticing that these architectures draw on concepts inherited from parallel and distributed systems to interconnect PEs in a structured and scalable way in order to achieve higher bandwidth and lower energy consumption when compared to conventional on-chip bus architectures. Furthermore, meeting

energy constraints is a prime requirement in NoC-based applications that typically run on battery operated devices [9]. Recently, we have proposed in [12,13] a new on-chip interconnect based on WK-recursive networks [14,29]. Since this on-chip interconnect has many attractive properties, such as high degree of regularity, symmetry and efficient communication, WK-Recursive networks have received considerable attention in parallel computing community [14]. In addition to these interesting properties that suit NoC, for any specified degree, it can be expanded to an arbitrary level without reconfiguring the edges. In addition to these qualitative features, we have compared, in [12,13], this architecture with 2D Mesh and the reported results show that WK-recursive interconnect generally outperforms 2D Mesh on-chip interconnect especially regarding the throughput, loss rate, communication load and the sensitivity for different traffic load models.

In this paper, we compare the energy consumption of the Wk-recursive on-chip interconnect with a regular 2D mesh on-chip interconnect since they present similar features in terms of scalability and performance. The rest of the paper is organized as follows. In section 2, we briefly survey existing work that intend to compare on-chip interconnect architectures in terms of energy consumption. Section 3 presents the proposed simulation methodology and reports the obtained results. Conclusion and further work are presented in section 4.

## II. RELATED WORK

NoC architectures adopted for MCSoC are characterized by different trade-offs with regard to latency, throughput, energy consumption, and silicon area requirements. These architectures have been extensively studied and compared based on different performance metrics such as message delay, throughput and communication load [7,17,20,21,22,23,26]. However, in the best of our knowledge, no much work have been done on energy consumption comparison for On-chip interconnect architectures. In [11], an energy model was proposed for NoC architectures based on packet and circuit switching techniques to predict their energy consumption per transported bit on the switches. A regular 2D mesh is compared with a traditional bus architecture using a complementary model proposed in [27] to estimate the energy consumption of the wires between the PEs. The reported results show that the energy required to transport one bit by the

bus-based architecture is higher than 2D mesh architecture. In addition, the energy consumption increases quickly as the number of PEs increases, so the benefit of using on-chip interconnect architectures is clearly visible for large MCSoCs. Moreover, the energy consumption when using the packet switching technique is a little bit higher than using circuit switching technique.

In [27], design methodologies and tools to assist designers in developing high performance and energy efficient NoC architectures were proposed. The objective was to optimize certain metrics such as minimizing the power and increasing the performance by customizing the given NoC platform for a specific application using an energy-aware scheduling algorithm. An energy model was also proposed and validated by simulation on a regular 2D mesh.

A consistent and meaningful simulation methodology was proposed in [7] to compare the performance characteristics of a variety of on-chip interconnect architectures, such as Fat-Tree, Butterfly-Fat Tree, 2D Mesh, Octagon, Torus, and F-Torus. Energy consumption model has been also proposed and simulation results have been reported because of the prime importance in SoC design. Area requirements as well as other performance metrics, such as message latency and throughput, were described. The reported results show that on-chip interconnect architectures with a higher degree of connectivity like 2D mesh and Octagon have greater average energy consumption at saturation point than the other architectures, but they provide higher throughput and lower latency on the average. In this paper, an energy model is introduced and simulation results are conducted to compare the energy consumption of the Wk-recursive on-chip interconnect architecture with 2D mesh architecture.

### III. SIMULATION METHODOLOGY

In this section, energy consumption for Wk-recursive and 2D mesh on-chip interconnects is evaluated using a simulator developed in [17]. This discrete event driven simulator is based on ns2 [24] that provides many facilities to describe network topology, transmission protocols, routing algorithms, and traffics generation. The main objective of using ns2 is to rapidly explore and evaluate the performance metrics as well as the energy consumption of on-chip interconnects.

#### A. Wk-recursive network: an overview

Wk-recursive network has received considerable attention in parallel community due to its many favorable properties, such as high degree of regularity, symmetry and efficient communication, scalability, and ease of extendibility [14]. One of the interesting properties of this structure that suits NoC is its ease of expandability [12,13]; the Wk-recursive network can be constructed hierarchically by grouping basic modules. More precisely, a Wk-Recursive network with amplitude  $W$  and level  $L$ , denoted by a  $WK(W,L)$ , can be recursively constructed [14]. A  $WK(W,0)$  is a vertex with  $W$  free edges. A  $WK(W,1)$  is a  $W$ -vertex complete graph that is denoted by a  $KW$ . Each vertex has one free edge and  $W-1$  edges that are

used for connecting to the other vertices. A  $WK(W,H)$  consists of  $W$  copies of  $WK(W,H-1)$  as supervertices and the  $W$  supervertices are connected as a  $KW$ , where  $2 \leq H \leq L$ . By induction,  $WK(W,L)$  has  $W^L$  vertices and  $W$  free edges. Consequently, for any specified degree  $W$ , Wk-Recursive networks can be expanded to an arbitrary level  $L$  without reconfiguring the edges. The structures of  $WK(4,0)$ , a  $WK(4,1)$ , and  $WK(4,2)$  are depicted in figure 1. More details about the Wk-recursive network features and topological properties can be found in [14,29,30].

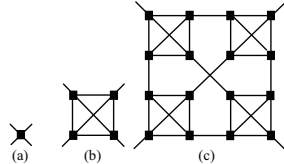


Fig.1. The structures of (a)  $WK(4,0)$ , (b)  $WK(4,1)$ , and (c)  $WK(4,2)$

Due to the qualitative properties of the Wk-recursive network, especially the ease of extendibility, that suits NoC systems, the rest of this paper studies and reports on energy consumption of same size 2D Mesh and Wk-recursive networks for NoC implementation.

#### B. Topology and traffic parameters

Figure 2 shows (a)  $WK(4,2)$ , (b) 2D mesh on-chip interconnects layout in the particular case of 16 PEs and 16 switches or routers. PEs are resources, such as processors, DSPs, and memory. These resources can be modeled as either source or sink in which messages are produced or consumed. As shown in this figure, there are two types of link, PE-to-switch and switch-to-switch. Two sorts of parameters are considered to model each link, link delay ( $d_l$ ) and maximal link capacity ( $B_{w_{max}}$ ). According to [25], the maximal bandwidth  $B_{w_{max}}$  for an on-chip communication link is expected to be in Gigabits. However, in this evaluation, the maximal link capacity is fixed to 200Mbps because of the amount resources (e.g., CPU, Memory) required to simulate heavy traffic load. The link delay is constant and independent from the network; increasing it will increase only the latency. This value is fixed to 0.1ms in this simulation. We consider also that the buffer size inside each PE is unlimited since it has enough space and speed to handle and process the arrived data preventing packets from dropping inside these nodes. In the switch, each port has a buffer for temporary storage of packets. When a packet arrives at a switch, it must go into the buffer. The buffer size is similar to a Drop-tail queue with FIFO queue management mechanism. In this type of queue, when the buffer capacity of the output queue is exceeded then the last packet to arrive will be dropped.

A deterministic routing protocol was used to direct flits between switches. Unlike dynamic routing protocols that require the implementation of a complex logic at the switch level, a deterministic routing protocol are usually used because

they require implementing a simple logic and therefore minimizes the silicon area inside the chip [22]. A wormhole switching technique should be used to decrease the packet drop problem, reduce the size of the buffer, and achieve a low latency. In [26], a way for ns2 to use wormhole technique instead of the store-and-forward technique is described, where flits are used instead of packets. In this technique, a packet is divided into elementary units, called flits, each composed of a few bytes for transmission and flow control [22]. The use of the ns2 simulator was also justified in [28] by comparing cycle accurate simulation using System-C with ns2 and proving that they have same behavior (i.e., results obtained are in the same order of magnitude).

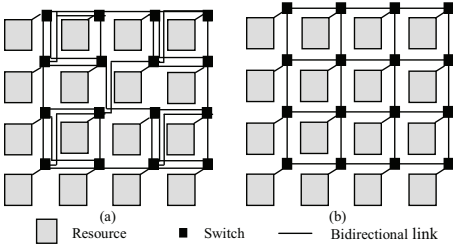


Fig.2. Chip layout of NoC Topologies: (a) WK (4,2), (b) 2D Mesh

We consider that the application is represented by communicating parallel processes. Each process is running on one PE and is linked with a traffic or workload generator that injects flits. Two methods were used to generate workload in the system. In the first method, we consider that PEs continually send data at a constant rate to the on-chip interconnect. In this method, the CBR (Constant Bit Rate) model was used to inject flits. The CBR model generates flits at a deterministic rate.

The second method employs probabilistic functions to model the applications' traffic behavior. Example of applications using this method is audio and video streams. In this second method, two kinds of traffic models were used to generate flits burst: Exponential and Pareto models. The exponential model is an ON/OFF model with exponential distributed ON and OFF times. During each ON period, an exponentially distributed random number of flits are generated at a fixed injection rate, with an average OFF time of 1ms, and an average ON time of 0.1s. In the Pareto model, four parameters are considered: the burst time, the idle time, the traffic rate (or injection rate), the size of the flits, and the shape. The burst time is the average ON time for the generator. The idle time is the average OFF time for the generator. The traffic rate is the injection rate during a period of ON time. During each ON period of the Pareto flow, flits are generated at fixed rate, an average burst time of 0.1s and an average idle time of 1ms. The shape parameter of the Pareto distributed OFF and ON times is 1.5. The values considered for the injection rate are

100, 130, 160, and 190 Mbps. The Pareto traffic generator was used by PEs to generate aggregate traffics that exhibits long range dependency [7,18,19]. In the reported results, the flit size is 8 bytes generated according to the traffic generator used.

At the beginning of each simulation instance, each source starts to generate flits according to the model used, CBR, Exponential, and Pareto. All PEs are traffic sources that transmit flits in order to simulate high traffic network load. However, sinks (destination PEs) are selected according to the following communication locality principle in which 75% of the traffic takes place between neighboring resources and 25% of the traffic is uniformly distributed among the rest [17]. In other words, 0.75 represents the probability of one PE being one hop away from PE selected as a sink, and 0.25 represents the probability of one PE being more than one hop away from the PE selected as a sink.

### C. Energy model

The total energy required to send one flit through the network can be decomposed into the energy consumed per hop (traversal of input and output switch) and energy consumed per wire, i.e., the distance traveled. Formally, the flit energy ( $E_{i,j}$ ) is defined as the energy consumed when one flit is sent through the source node  $PE_i$  to a destination node  $PE_j$ . It can be calculated as follows:

$$E_{i,j} = hE_L + (h-1)E_R \quad (1)$$

where  $h$  is the number of links the flit crosses,  $E_L$  is the average energy consumed during transporting the flit between two neighboring PEs, and  $E_R$  is the average energy consumed during buffering and routing operations inside the switch. The values of  $E_L$  and  $E_R$  are constants for a given on-chip interconnect and depend mainly on the switch architecture and the link characteristic such as the width, the length, etc [27]. Based on equation 1, the total energy consumed by all flits can be calculated as follows:

$$E = \sum_{k=1}^{Nb_f} (h(k)E_L + (h(k)-1)E_R) \quad (2)$$

where,  $h(k)$  is the number of links the flits  $k$  passes and  $Nb_f$  is the total number of generated flits. The values  $E_L$  and  $E_R$  are calculated based on the model proposed in [11]. In this model, the amount of energy required for a single bit to pass the switch is equal to 0.9776 pJ/bit and the amount of energy required for a single bit to cross a link is  $(0.39 + 0.12 \times \ell_w)$  pJ/bit, where  $\ell_w$  is the length of the link. Therefore, the average energy is calculated from equation (2) as:

$$E_{av} = Nb_f S_f (h_{av} (0.39 + 0.12 \times \ell_w^{av}) + 0.9776 (h_{av} - 1)) \quad (3)$$

where  $h_{av}$  is average number of links traversed by all flits sent by PEs,  $S_f$  is the size of the flit and  $\ell_w^{av}$  is the average link

length. We can see that the energy consumption depends mainly on the application traffic ( $Nb_f$ ), the number of hops or links that flits traverse ( $h_{av}$ ), and the average link length ( $\ell_W^{av}$ ). To show the impact of these parameters on the energy consumption, we select different communication loads and three types of traffic generators that imitate three types of applications.

#### D. Simulation results

Different simulation scenarios for each on-chip architecture are performed and the energy consumption was evaluated. Different values of the injection rate from light traffic to heavy traffic are considered (100, 130, 160, and 190Mbps). The values of the buffer size considered in the simulation are 2, 4, 8, 16, and 32 flits. The size of each flit is considered constant in this simulation (8 bytes). To evaluate the average energy consumption, we have to calculate the average link length  $\ell_W^{av}$  of each on-chip interconnect based on its on-chip layout as

depicted in figure 1. In addition, the link length is evaluated based on the assumption that all resources and switches are placed on a 2-D regular substrate with x- and y-directions. In both architectures, we consider that the link between each PE (resource) and its corresponding switch is of length  $\ell_W^r$  equal to 1mm. Both architectures, as depicted in figure 1, have 16 links of length  $\ell_W^r$  but the length of links between neighboring switches is calculated based on its on-chip layout. All links (horizontal or vertical) between neighboring switches, at  $1, 2, \dots, i, \dots, n$  hops, when placed on the 2-D regular substrate are also considered to be of length  $\ell_W^{s1}, \ell_W^{s2}, \dots, \ell_W^{si}, \dots, \ell_W^{sn}$  respectively, where  $\ell_W^{si} = 2 \times i$  mm. As shown in figure 1, the mesh has 16 links of length  $\ell_W^r$ , 24 links of length  $\ell_W^{s1}$ , so the average length is 1.6 mm. The Wk-recursive network has 16 links of length  $\ell_W^r$ , 20 links of length  $\ell_W^{s1}$  and 10 links of length  $\ell_W^{s2}$ , so the average link length is 2.087 mm.

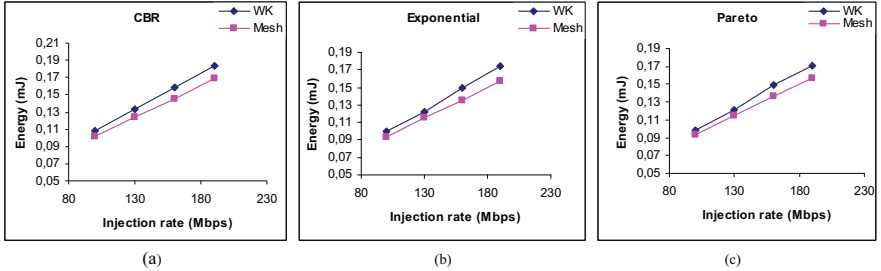


Fig.3. Average energy consumption: (a) CBR, (b) Exponential, (c) Pareto

At the end of each simulation instance, ns2 generates several data (i.e., a trace file). Each line in the trace file contains the following information: event (enqueue (+), dequeue (-), receive (r), or drop (d)), the current time (in second), traffic source, traffic sink, type of packet (e.g., CBR), flit size (bytes), flags flow identifier, source and destination nodes in form of "node.port", flit sequence number, and unique identifier of the flit. Having simulation trace data at hand, we can transform a subset of the data of interest into comprehensible information and analyze it. For example, we can calculate the number of flits sent or received by nodes, the number of flits dropped, the average latency, the number of hops, etc. According to the energy model, the energy consumption depends mainly on the application traffic (number of generated flits), the number of hops or links that the flits traverse. Since from the trace file, we can calculate the average number of hops and the number of flits generated, so we can evaluate the average energy consumption.

In equation (3), since the values of  $S_{flit}$  and  $\ell_W^{av}$  are constants, so the average energy consumption depends mainly on the average number of hops traversed by the flits and the

number of flits injected and cross the network. Let's now examine the influence of the injection rate on the energy consumption. The results depicted in figure 3 compare the energy consumption of these two on-chip architectures in function of the injection rate when the CBR (a), Exponential (b), and Pareto (c) models are used and under different traffic rates (the buffer size is fixed here to 16 flits). This figure (3-a, 3-b, 3-c) shows that Wk-recursive interconnect has highest energy consumed compared to the 2D mesh for the three traffic generator models.

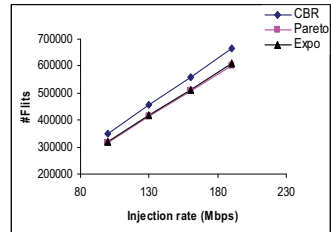


Fig. 4. Number of flits generated in function of the injection rate

In addition, the average energy consumption increases when the injection rate increases. This can be explained by the big number of flits generated as the injection rate increases as shown in figure 4. We can also see, in this figure, that the number of flits generated when using the CBR model is higher in comparison with the Exponential and Pareto models. This is the reason why the average energy consumption using CBR (for both architectures) is higher in comparison with the energy consumption when using the Exponential and Pareto models.

To explain now the reason why the energy consumption in WK-recursive on-chip interconnects is higher than the energy consumption in 2D mesh, we have to compare the number of hops in both architectures. Figure 5 compares the average number of hops in function of the injection rate when CBR (a), Exponential (b), and Pareto (c) models are used. This figure

shows that the average number of hops, for all flits dropped or arrived to the destinations, decreases when the injection rate increases. Moreover, WK-recursive interconnect shows highest number of hops compared to the 2D mesh in the three traffic generator models.

We conclude from this figure that the number of hops influences on the energy consumption. Even the average number of hops decreases as the injection rate increases the average energy consumption increases. It is worth noticing that the number of hops is not only the factor that influence the higher energy consumption in WK-recursive on-chip interconnect, but also the flits that traverse the network and not dropped. As the injection rate increases the network becomes more congested with heavy traffic and so queues become full causing more flits to drop.

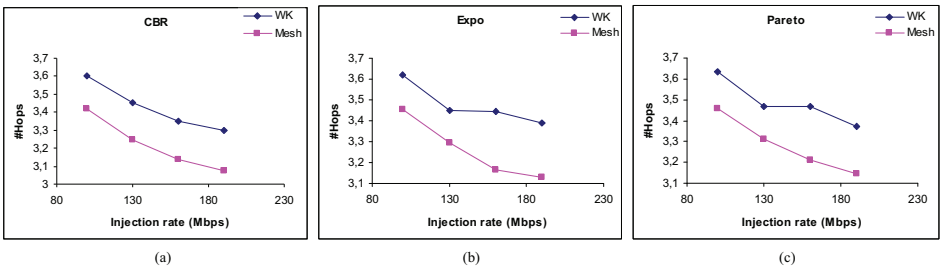


Fig. 5. Average number of hops: (a) CBR, (b) Exponential, (c) Pareto

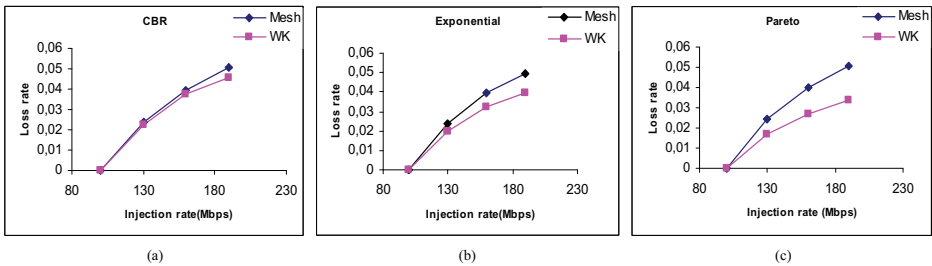


Fig. 6. Comparison of WK and Mesh by variation of loss rate vs. injection rate: (a) CBR, (b) Exponential, (c) Pareto

Figure 6 illustrates the variation of loss rate under different injection rate values when CBR (a), Exponential (b), and Pareto (c) traffics are used. Independent of the traffic generator considered, WK has lower sensitivity than the 2D mesh so more flits cross the network and more energy are consumed (see figure 3-a, 3-b, and 3-c). It is clear in figure 6 that keeping the data rate half (100 Mbps) of the available bandwidth reduces flits drop to zero with a buffer size of 16 flits at each switch. This is the reason why the average energy consumption for Wk-recursive on-chip interconnect is little bit higher in comparison with energy consumed by 2D mesh

architecture. In this rate, the average number of hops is only the big factor that influences this small difference. Similar results were produced for the rest of architectures by varying the buffer size (2, 4, 8, and 32 flits). However, we choose not to show them here because of similar behavior as in Figures 3, 5 and 6 and the number of page limitation as well.

It is worth noticing that the main objective of this high level simulation study is to evaluate different patterns on relatively large number of PEs, which might be difficult to realize with real hardware and system level simulation, but we are in the stage of implementing this study in smaller system for proof of

concept. This ongoing study will also allow us to evaluate the silicon area consumed by all components (Control logic, buffers, PEs, links, etc).

#### IV. CONCLUSIONS AND FUTURE WORK

In this paper, we quantitatively evaluated the average energy consumption of the proposed on-chip interconnect based on the WK recursive network for different communication load and traffic models. The study compares this architecture with another similar NoC architecture, the 2D regular mesh. We investigated the effects of load and traffic models and the obtained results show that the traffic models and load that ends PEs generate has a direct effect on the energy consumption. In these results, WK-recursive interconnect generally has a higher energy consumption in all load and traffic models.

The energy consumption comparison of these two on-chip interconnects when using circuit-switching technique is under investigation. Future work addresses the comparison based on area overhead and wiring complexity of the Wk-recursive and 2D mesh on-chip interconnects. The objective is to determine the amount of relative silicon area they require in function of switches and PEs size.

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